CLAIMS

1. A circuit architecture for buses, comprising: encoder/decoder architecture for buses, capable of receiving a current value of input information relating to a given instant and of generating, from this current input value, a corresponding output value relating to the same given instant on encoded bus lines, the encoder/decoder architecture comprising:

at least one memory element for storing the respective preceding input information value and output information value,

a prediction block for generating an estimate of the current input information value on the basis of the preceding input information value, and

a decorrelation block for decorrelating the current input information value with respect to the estimate, to produce a decorrelation result,

the current output value adapted to be selected as one of the following:

the current input information value,

the preceding output value, and

the decorrelation result.

2. The architecture of claim 1, comprising a selection block for selecting the current output value.

3. The architecture of claim 1 wherein the at least one memory element comprises corresponding registers for storing the corresponding preceding input information values and output information values.

4. The architecture of claim 1 wherein at least one of the blocks is at least partially implemented by means of pass-gates.

5. The architecture of claim 1, comprising:

a redundant line, preferably configured to transfer information on the sequentiality of the information, acting as a prediction block,

an XOR logic gate, acting as a decorrelation block, and

a multiplexer, acting as a selection block for selecting the current output value.

6. The architecture of claim 5 wherein the selection block comprises an inverter and a pass-gate.

7. The architecture of claim 1, comprising:

an identity module, acting as a prediction module,

a decorrelation block, acting as an XOR logic gate, and

an inverter, acting as a selection block for selecting the current output value.

8. The architecture of claim 1, comprising:

one of either a redundant line, preferably configured for transferring information on the sequentiality of the said information, and an identity module, acting as a prediction module,

an XOR logic gate, acting as a decorrelation block, and

one of either a multiplexer and an inverter, acting as a selection block for selecting the said current output value.

9. The architecture of claim 1, comprising:

a redundant line, preferably configured for transferring information on the sequentiality of the information, acting as a prediction module,

an XOR logic gate, acting as a decorrelation block, and

an XOR logic gate, acting as a selection block for selecting the current output value.

10. The architecture of claim 9 wherein the selection block comprises an inverter and a pass-gate.

11. The architecture of claim 1, comprising:

an identity module, acting as a prediction module, and

a difference module, acting as a decorrelation block, which is also capable of selecting the current output value.

12. The architecture of claim 1, comprising:

an identity module, acting as a prediction module, and

a difference module, acting as a decorrelation block, and

an XOR logic gate, acting as a selection block capable of selecting the said current output value.

13. The architecture of claim 1, comprising:

one of either a redundant line, preferably configured for transferring information on the sequentiality of the said information, and an identity module, acting as a prediction module,

one of either an XOR logic gate and a difference module, acting as a decorrelation block, and

a multiplexer, acting as a selection block for selecting the said current output value.

14. The architecture of claim 1, comprising:

one of either a redundant line, preferably configured for transferring information on the sequentiality of the information, and an identity module, acting as a prediction module,

one of either an XOR logic gate and a difference module, acting as a decorrelation block, and

an XOR logic gate, acting as a selection block for selecting the said current output value.

15. A processing system, comprising a bus and at least one bus interface capable of receiving a current value of input information relating to a given instant and of generating, from this current input value, a corresponding output value relating to the same given instant on encoded bus lines, the encoder/decoder architecture comprising:

at least one memory element for storing the respective preceding input information value and output information value,

a prediction block for generating an estimate of the current input information value on the basis of the preceding input information value, and

a decorrelation block for decorrelating the current input information value with respect to the estimate, to produce a decorrelation result,

the current output value adapted to be selected as one of the following:

the current input information value,

the preceding output value, and

the decorrelation result.

16. The system of claim 15 wherein the at least one bus interface operates at sub-system level.

17. The system of claim 16 wherein the at least one bus interface operates at the processor-to-cache bus level.

18. The system of claim 15 wherein the at least one bus interface operates at system level.

19. The system of claim 15, configured in the form of a shared memory multiprocessor system.

20. The system of claim 15, comprising a structure of the monolithic type.

21. The system of claim 15, comprising a structure of the multichip type.

22. A bus interface for a bus, comprising:

an input for receiving a current input information value;

at least one register coupled to the input to receive and store a respective preceding input information value and coupled to an output to store a preceding output value;

a prediction block coupled to the registers and configured to generate an estimate of the current input information value based on the preceding input information value;

a decorrelation block coupled to the input and the prediction block and configured to decorrelate the current input information value with respect to the estimate and to generate a decorrelation result; and

a selection block coupled to the input and the decorrelation block and configured to select a current output value from one of the current input information value, the decorrelation result, and the preceding output value.

23. The interface of claim 22 wherein the prediction block comprises a redundant line configured to transfer information on the sequentiality of received input information valve; the decorrelation block comprising an XOR logic gate; and the selection block comprising a multiplexer configured to select the current output value.

24. The interface of claim 22 wherein the prediction module comprises an identity module; the decorrelation block comprises an XOR logic gate; and the selection block comprises an inverter configured to select the current output value.

25. The interface of claim 22 wherein the prediction block comprises one of either a redundant line, preferably configured for transferring information on the sequentiality of received input information valve, and an identify module; the decorrelation block comprising an

XOR logic gate; and the selection block comprising one of either a multiplexer and an inverter configured to select the current output value.

26. The interface of claim 22 wherein the prediction block comprises a redundant line configured for transferring information on the sequentiality of the received input information valve; the decorrelation block comprising an XOR logic gate; and the selection block comprising an XOR logic gate configured to select the current output value.

27. The interface of claim 22 wherein the prediction block comprises an identity module, and the decorrelation block comprises a difference module configured to also select the current output value.

28. The interface of claim 22 wherein the prediction block comprises an identity module; the decorrelation block comprises a difference module; and the selection block comprises an XOR logic gate configured to select a current output value.

29. The interface of claim 22 wherein the prediction block comprises one of either a redundant line configured for transferring information on the sequentiality of received information and an identity module; the decorrelation block comprises one of either an XOR logic gate and a difference module; and the selection block comprises a multiplexer configured to select a current output value.

30. The interface of claim 22 wherein the prediction block comprises one of either a redundant line configured for transferring information on the sequentiality of received input information valve and an identity module; the decorrelation block comprising one of either an XOR logic gate and a difference module; and the selection block comprising an XOR logic gate configured to select the current output value.